In the claims:

1. (original) A chip module for an emulation system, comprising:

a plurality of cells logically arranged in S rows and P columns, each row corresponding to a wave, each cell comprising:

(a) a plurality of input lines,

(b) a configurable logic function memory element specifying a logic function of said plurality of input lines, and

(c) a logic function element performing the logical function specified by said configurable logic function memory element on said plurality of input lines to produce an output;

configurable interconnection logic, said configurable interconnection logic routing the output of any cell to an input of any other cell; and

wave logic for producing a plurality of sequential wave signals, each wave signal corresponding to a row of cells and controlling the propagation of logic signals through the cells of the row.

2. (original) The chip module of claim 1, wherein said configurable interconnection logic comprises a time-multiplexed array of interconnections controlled by an interconnection control memory, said interconnection control memory having a plurality of entries, one entry corresponding to each wave of said wave logic, wherein interconnection of each wave are specified by the corresponding entry in said interconnection control memory.

3. (original) The chip module of claim 1, wherein said wave logic includes delay logic for delaying the generation of an Nth sequential wave signal if an output required to be transmitted to an external source before generation of said Nth sequential wave signal has not yet been transmitted.

4. (original) The chip module of claim 1, wherein said wave logic includes delay logic for delaying the generation of an Nth sequential wave signal if an input required to be received from an external source before generation of said Nth sequential wave signal has not yet been received.

5. (original) The chip module of claim 1, further comprising a set of P output ports for transmitting data external to said chip module, each output port of said set corresponding to a respective column of cells, wherein each output port of said set is shared by the cells in the respective corresponding column of cells on a time-multiplexed basis.

6. (original) The chip module of claim 5, wherein each output port of said set of P output ports comprises a data line and a strobe line, said strobe line indicating when data is available on said data line.

7. (original) The chip module of claim 1, further comprising a set of P input ports for receiving data from at least one source external to said chip module, each input port of said set corresponding to a respective column of cells, wherein each input port of said set is shared by the cells in the respective corresponding column of cells.

8. (original) The chip module of claim 7, wherein each input port of said set of P input ports comprises a data line and a strobe line, said strobe line indicating when data is available on said data line.

9. (original) An emulation engine, comprising:

a plurality of interconnected emulation boards;

a plurality of chip modules mounted on said emulation boards, each board containing multiple chip modules, each chip module containing:

(a) a plurality of cells logically arranged in S rows and P columns, each row corresponding to a wave, each cell comprising:

(iv) a plurality of input lines,

(v) a. configurable logic function memory element specifying a logic function of said plurality of input lines, and

(vi) a logic function element performing the logical function specified by 11 said configurable logic function memory element on said plurality of input lines to produce an output;

(b) configurable interconnection logic, said configurable interconnection logic routing the output of any cell to an input of any other cell; and

(c) wave logic for producing a plurality of sequential wave signals, each wave signal corresponding to a row of cells and controlling the propagation of logic signals through the cells of the row.

10. (original) The emulation engine of claim 9, wherein said configurable interconnection logic comprises a time-multiplexed array of interconnections controlled by an

interconnection control memory, said interconnection control memory having a plurality of entries, one entry corresponding to each wave of said wave logic, wherein interconnection of each wave are specified by the corresponding entry in said interconnection control memory.

11. (original) The emulation engine of claim 9, wherein said wave logic includes delay logic for delaying the generation of an Nth sequential wave signal if an output required to be transmitted to an external source before generation of said Nth sequential wave signal has not yet been transmitted.

12. (original) The emulation engine of claim 9, wherein said wave logic includes delay logic for delaying the generation of an Nth sequential wave signal if an input required to be received from an external source before generation of said Nth sequential wave signal has not yet been received.

13. (original) The emulation engine of claim 9, wherein each chip module further comprises:

(iv) a set of P output ports for transmitting data external to said chip module, each output port of said set corresponding to a respective column of cells, and

(v) a set of P input ports for receiving data from a source external to said chip module, each input port of said set corresponding to a respective column of cells,

wherein each output port of said set is mapped to a single input port of said set in another chip module in a one-to-one correspondence.

14. (original) The emulation engine of claim 13, wherein each output port of said set of P output ports and each input port of said set of P input ports comprises a data line and a strobe line, said strobe line indicating when data is available on said data line.

15. (New) The chip module of claim 9, further comprising a set of P input ports for receiving data from at least one source external to said chip module, each input port of said set corresponding to a respective column of cells, wherein each input port of said set is shared by the cells in the respective corresponding column of cells.

16. (New) The chip module of claim 15, wherein each input port of said set of P input ports comprises a data line and a strobe line, said strobe line indicating when data is available on said data line.